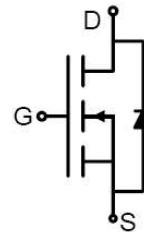


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Features

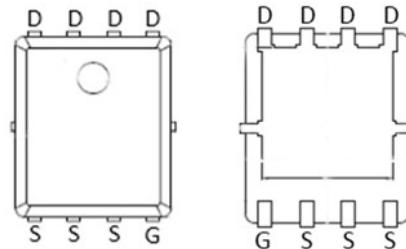
- 40V,50A
 - $R_{DS(ON)}=5.9\text{m}\Omega$ (Typ.) @ $V_{GS} = 10\text{V}$
 - $R_{DS(ON)}=11\text{m}\Omega$ (Typ.) @ $V_{GS} = 4.5\text{V}$
- High Density Cell Design for Ultra Low $R_{DS(ON)}$
- Fully Characterized Avalanche Voltage and Current
- Good Stability and Uniformity with High E_{AS}
- Excellent Package for Good Heat Dissipation



Schematic Diagram

Application

- Load Switch
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



PDFN5X6-8L

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		40	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current	$T_C = 25^\circ\text{C}$	50	A
		$T_C = 100^\circ\text{C}$	34	A
I_{DM}	Pulsed Drain Current ^{note1}		200	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}		196	mJ
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	42	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case		3.0	$^\circ\text{C}/\text{W}$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$

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Electrical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=40\text{V}, V_{GS}=0\text{V},$	-	-	1.0	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.0	1.5	2.5	V
$R_{\text{DS}(\text{on})}$ note3	Static Drain-Source on-Resistance	$V_{GS}=10\text{V}, I_D=30\text{A}$	-	5.9	7.5	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}, I_D=20\text{A}$	-	11	14	
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}, I_D=15\text{A}$	10	27	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=20\text{V}, V_{GS}=0\text{V}, f=1.0\text{MHz}$	-	2229	-	pF
C_{oss}	Output Capacitance		-	187	-	pF
C_{rss}	Reverse Transfer Capacitance		-	167	-	pF
Q_g	Total Gate Charge	$V_{DS}=20\text{V}, I_D=30\text{A}, V_{GS}=10\text{V}$	-	48	-	nC
Q_{gs}	Gate-Source Charge		-	6	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	13	-	nC
Switching Characteristics						
$t_{d(\text{on})}$	Turn-on Delay Time	$V_{DD}=20\text{V}, I_D=30\text{A}, R_L=1\Omega, R_{\text{GEN}}=3\Omega, V_{GS}=10\text{V}$	-	13	-	ns
t_r	Turn-on Rise Time		-	37	-	ns
$t_{d(\text{off})}$	Turn-off Delay Time		-	46	-	ns
t_f	Turn-off Fall Time		-	15	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	50	-	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	200	-	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS}=0\text{V}, I_S=30\text{A}$	-	-	1.2	V
t_{rr}	Body Diode Reverse Recovery Time	$T_J=25^\circ\text{C}, I_F=20\text{A}, dI/dt=100\text{A}/\mu\text{s}$	-	15	-	ns
Q_{rr}	Body Diode Reverse Recovery Charge		-	6	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: $T_J=25^\circ\text{C}$, $VG=10\text{V}$, $RG=25\Omega$, $L=0.5\text{mH}$

3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$

Typical Performance Characteristics

Figure 1: Output Characteristics

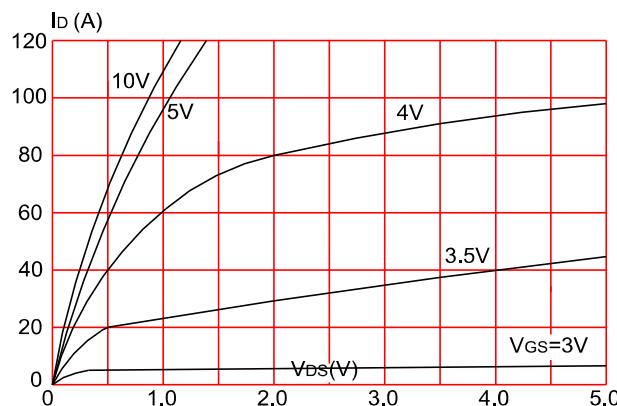


Figure 2: Typical Transfer Characteristics

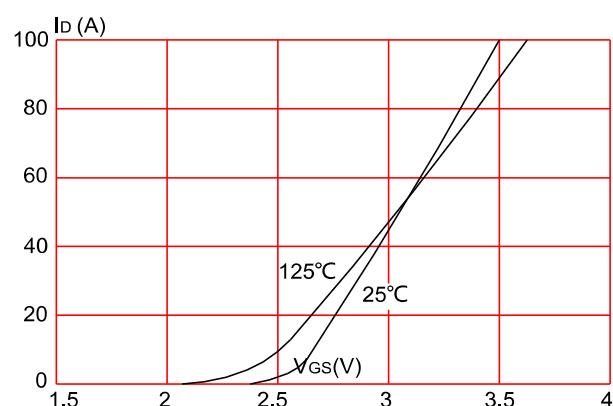


Figure 3: On-resistance vs. Drain Current

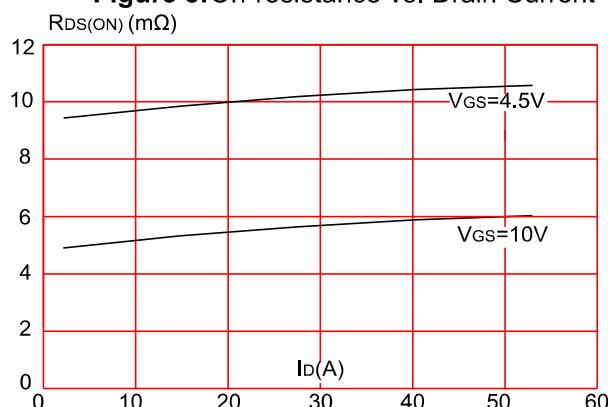


Figure 5: Gate Charge Characteristics

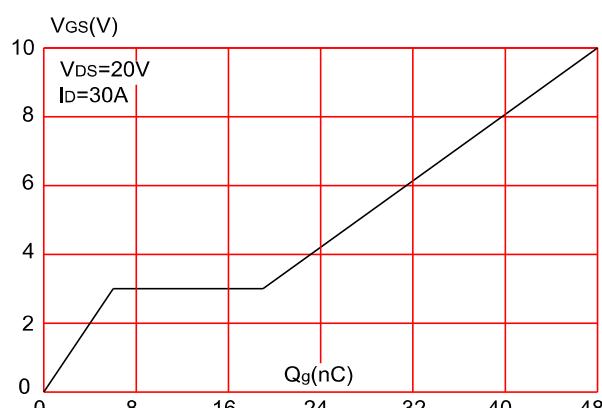


Figure 4: Body Diode Characteristics

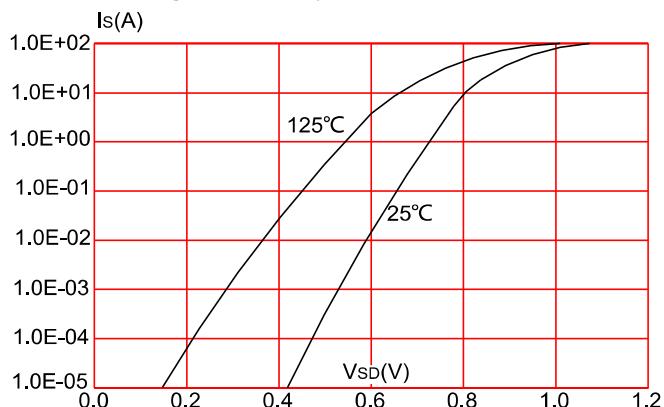
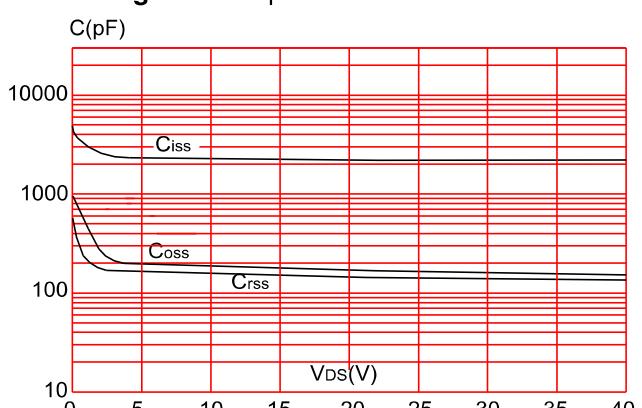


Figure 6: Capacitance Characteristics



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Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

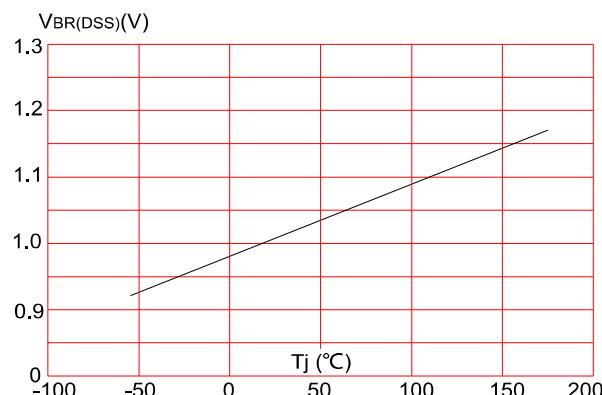


Figure 8: Normalized on Resistance vs. Junction Temperature

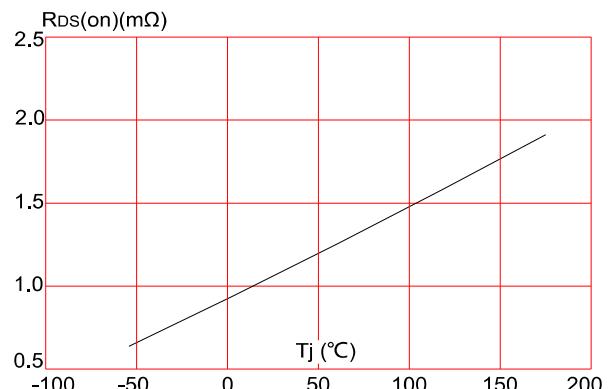


Figure 9: Maximum Safe Operating Area

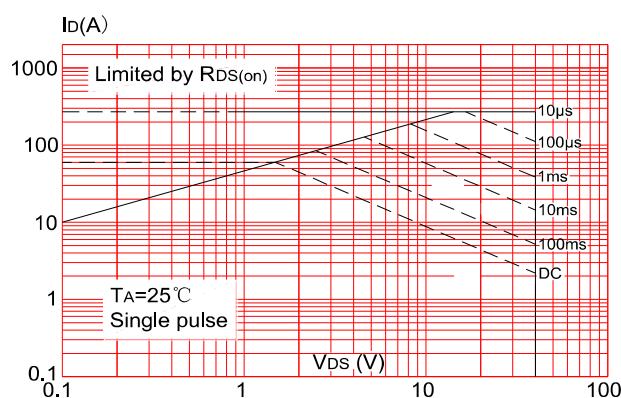


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case (PDFN3.3*3.3-8L)

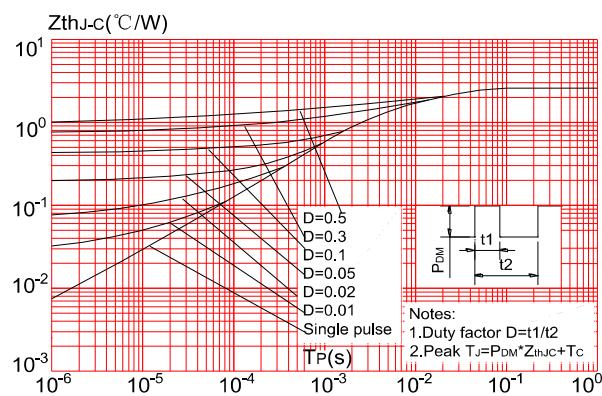
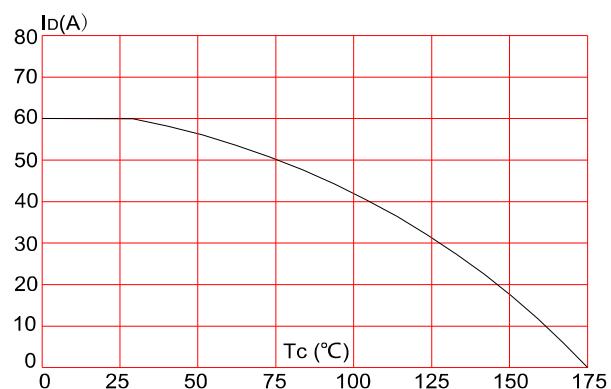


Figure 10: Maximum Continuous Drain Current vs. Case Temperature



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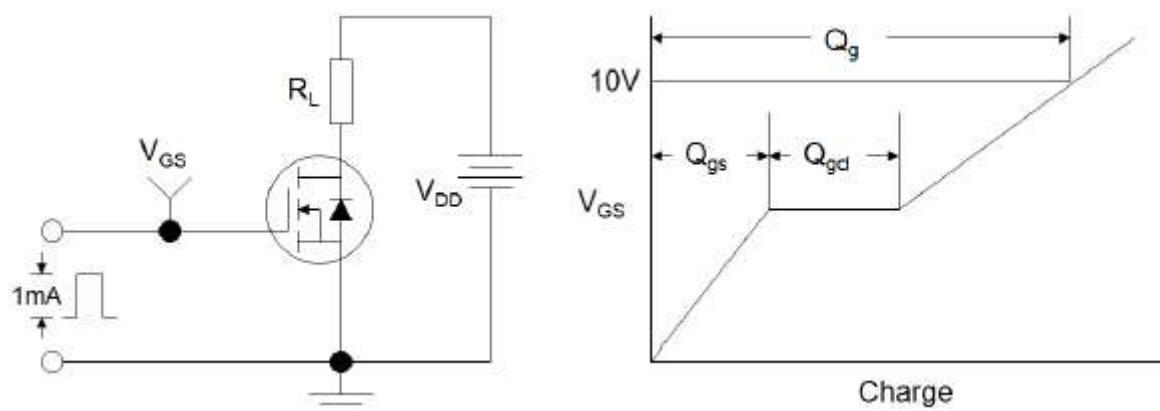


Figure 1: Gate Charge Test Circuit & Waveform

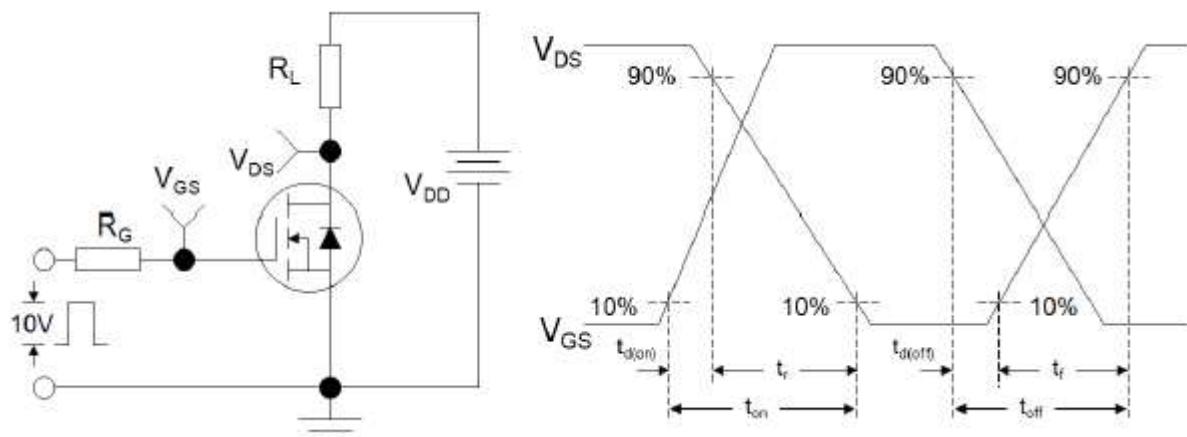


Figure 2: Resistive Switching Test Circuit & Waveforms

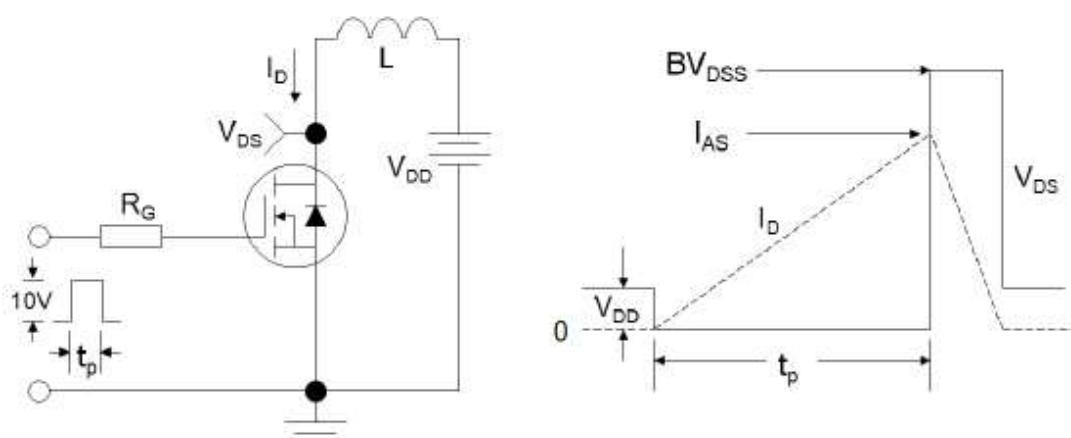


Figure 3: Unclamped Inductive Switching Test Circuit & Waveforms

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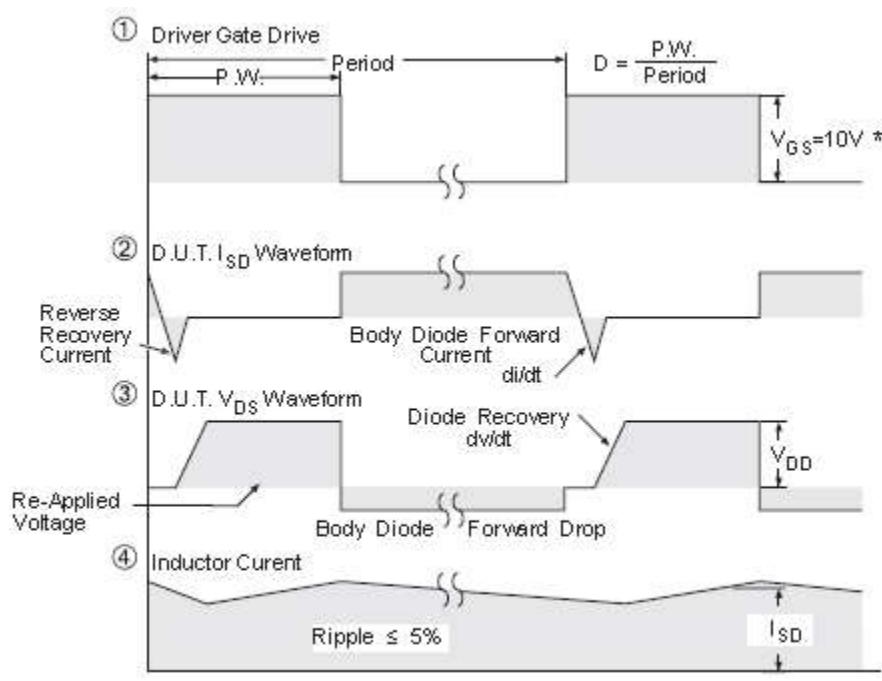
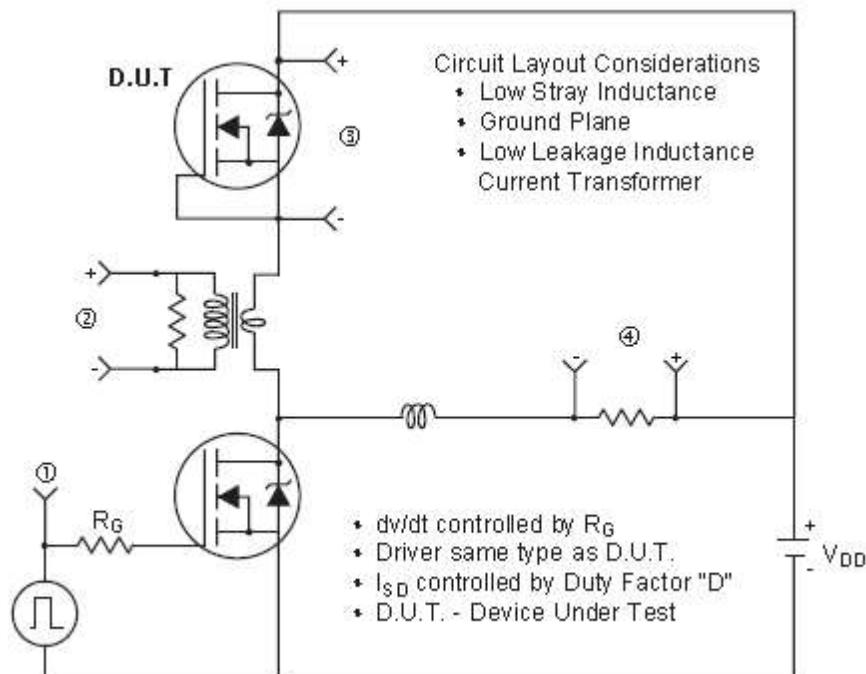
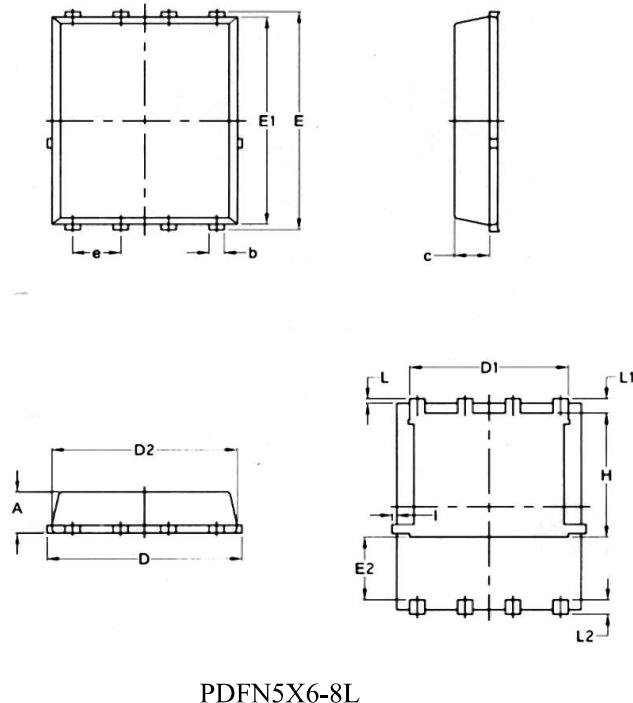


Figure 4:Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

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Package Mechanical Data



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SYMBOL	COMMON			
	MM		INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.970	0.0324	0.0382
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	—	0.0630	—
e	1.27	BSC	0.05	BSC
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	—	0.18	—	0.0070